Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of the claims in the application:

Listing of Claims:

1. (Original) An apparatus, comprising:

a variable speed bus;

a first unit coupled to the variable speed bus;

a second unit coupled to the variable speed bus; and

an arbitration and bus clock control unit to adjust the variable speed bus frequency depending on the bandwidth requirements of the first and second units, the arbitration and bus clock control unit to monitor which of the first and second units are active and to select an appropriate arbitration configuration depending on which of the first and second units are active.

2. (Original) The apparatus of claim 1, wherein the first unit is a host processor unit.

3. (Original) The apparatus of claim 1, wherein the second unit is a video processor unit.

4. (Original) The apparatus of claim 1, wherein the first unit is a graphics processor unit.

5. (Original) The apparatus of claim 1, wherein the second unit is a peripheral device controller unit.

6. (Original) The apparatus of claim 1, wherein the variable speed bus, the first unit, the second unit, and the arbitration and clock control unit are located on a single semiconductor die.

7. (Original) A system, comprising:

a variable speed bus;

a first device coupled to the variable speed bus;

a memory coupled to the variable speed bus;

a second device coupled to the variable speed bus; and

an arbitration and bus clock control unit to adjust the variable speed bus frequency depending on the bandwidth requirements of the first and second devices, the arbitration and bus clock control unit to monitor which of the first and second devices are active and to select an appropriate arbitration configuration depending on which of the first and second devices are active.

8. (Currently amended) The system of claim 7 [[10]], wherein the first device coupled to the variable speed bus is a processor.

9. (Original) The system of claim 8, wherein the second device coupled to the variable speed bus is a video processor.

10. (Original) The system of claim 9, further comprising a third device coupled to the variable speed bus, the arbitration and bus clock control unit to monitor whether the third device is active and to select an appropriate arbitration configuration depending on which of the first, second, and third devices are active.

11. (Original) The system of claim 10, wherein the third device coupled to the variable speed bus is a peripheral device controller.

12. (Original) The system of claim 11, the variable speed bus being 64 bits in width.

13. (Original) A method, comprising:

determining which of a plurality of units coupled to a variable speed bus are active;

adjusting the clock frequency of the variable speed bus according to the bandwidth requirements of the active units; and

selecting one of a plurality of arbiter configurations depending on which of the plurality of units coupled to the variable speed bus are active.

14. (Original) The method of claim 13, wherein determining which of a plurality of units coupled to a variable speed bus are active includes determining which of a host processor, a graphics processor, a peripheral device controller, and a video processor are active.

15. (Original) The method of claim 14, wherein adjusting the clock frequency of the variable speed bus includes setting the clock frequency to a first frequency if the host processor and the graphics controller are determined to be inactive.

16. (Original) The method of claim 15, wherein selecting one of a plurality of arbiter configurations includes selecting a first configuration if the host processor and the graphics processor are determined to be inactive.

17. (Original) The method of claim 14, wherein adjusting the clock frequency of the variable speed bus includes setting the clock frequency to a second frequency if the host processor and the graphics controller are determined to be active.

18. (Original) The method of claim 17, wherein selecting one of a plurality of arbiter configurations includes selecting a second configuration if the host processor and the graphics processor are determined to be active.